Abstract of the Disclosure

A power-up circuit of a semiconductor memory device includes a power supply voltage level follower unit for providing a bias voltage which is linearly varied according to variation of a power supply voltage, a power supply voltage detection unit for detecting the variation of the power supply voltage to a predetermined critical voltage level in response to the bias voltage, and a reset prevention unit for canceling variation of the detection signal due to a power drop by delaying level transition of the detection signal according to decrease of the power supply voltage.